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Nuno Marques , Mattan Kamon , Jacob White , L. Miguel Silveira
Proceedings of the 35th annual conference on Design automation conference May 1998
 As VLSI circuit speeds have increased, reliable chip and system design can no longer be performed without accurate three-dimensional interconnect models. In this paper, we describe an integral equation approach to modeling the impedance of inter-connect structures accounting for both the charge accumulation on the surface of conductors and the current traveling in their interior: Our formulation, based on a combination of nodal and mesh analysis, has the required properties to be combined wi ...
- 2** Drawing graphs to convey proximity: an incremental arrangement method 80%

Jonathan D. Cohen
ACM Transactions on Computer-Human Interaction (TOCHI) September 1997
 Volume 4 Issue 3
 Graph drawings are increasingly finding their way into user interfaces to convey a variety of relationships. This article deals with rendering graphs to show proximity between vertices by making their configuration (screen) distances reflect their distances in the graph. An arrangement method is described that achieves good drawings at speeds suitable for user interaction on a desktop computer. The method is "incremental" in that it first arranges a small portion of the graph, t ...
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David Campbell , Doyne Farmer , Jim Crutchfield , Erica Jen
Communications of the ACM April 1985
 Volume 28 Issue 4
 Computers have expanded the range of nonlinear phenomena that can be explored mathematically. An "experimental mathematics facility," containing both special-purpose dedicated machines and general-purpose mainframes, may someday provide the ideal context for complex nonlinear problems.
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Anthony C. Hearn
Proceedings of the second ACM symposium on Symbolic and algebraic manipulation March 1971
 This paper surveys the applications of symbolic computation techniques to problems in theoretical physics. Particular emphasis is placed on applications in quantum electrodynamics where the most activity has occurred.
- 5** An efficient algorithm for fast parasitic extraction and passive order reduction of 3D interconnect models 77%

N. Marques , M. Kamon , J. White , L. M. Silveira
Proceedings of the conference on Design, automation and test in Europe February 1998
 As VLSI circuit speeds have increased, the need for accurate three-dimensional interconnect models has become essential to accurate chip and system design. In this paper, we describe an integral equation approach to modeling the impedance of interconnect structures accounting for both the charge accumulation on the surface of conductors and the current traveling along conductors. Unlike previous methods, our approach is based on a modified nodal analysis formulation and can be used directly to g ...
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Anthony C. Hearn
Communications of the ACM August 1971
 Volume 14 Issue 8

This paper surveys the applications of symbolic computation techniques to problems in theoretical physics. Particular emphasis is placed on applications in quantum electrodynamics where the most activity has occurred.

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Donald E. Knuth
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Volume 15 Issue 8
- 8** The cosmic cube 77%
Charles L. Seitz
 **Communications of the ACM** January 1985
Volume 28 Issue 1
Sixty-four small computers are connected by a network of point-to-point communication channels in the plan of a binary 6-cube. This "Cosmic Cube" computer is a hardware simulation of a future VLSI implementation that will consist of single-chip nodes. The machine offers high degrees of concurrency in applications and suggests that future machines with thousands of nodes are both feasible and attractive.
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 Vincenzo Piuri
Proceedings of the 24th annual symposium on Simulation April 1991
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 Harold Abelson , Michael Eisenberg , Matthew Halfant , Jacob Katzenelson , Elisha Sacks , Gerald J. Sussman , Jack Wisdom , Ken Yip
Communications of the ACM May 1989
 Volume 32 Issue 5
 The authors discuss the development of intelligent techniques appropriate for the automatic preparation, execution, and control of numerical experiments.
- 3** NONLISA: Nonlinear network simulation and analysis program 80%
 Toru Tsuda , Takuhito Kojima , Shinji Goto , Toshihiko Nakamura
Proceedings of the June 1971 design automation workshop on Design automation June 1971
 Many programs for analyzing electronic circuits including nonlinear elements have been reported. It became difficult to evaluate circuits such as ICs by the breadboard method, because this method is not always suitable for simulation of high speed and high density circuits. Moreover lengthy experiments are involved. In the case of circuits composed of discrete parts, it was considered that many manual experiments could be replaced by computer aided analysis. We developed a general nonlinear ...
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 J. T. Deutsch , A. R. Newton
Papers on Twenty-five years of electronic design automation June 1988
- 5** IFIP Congress-62, Munich, Germany, August 27-September 1, 1962: Abstracts of papers 80%
Communications of the ACM June 1962
 Volume 5 Issue 6
- 6** A case study in programming for parallel-processors 80%
 Jack L. Rosenfeld
Communications of the ACM December 1969
 Volume 12 Issue 12
 An affirmative partial answer is provided to the question of whether it is possible to program parallel-processor computing systems to efficiently decrease execution time for useful problems. Parallel-processor systems are multiprocessor systems in which several of the processors can simultaneously execute separate tasks of a single job, thus cooperating to decrease the solution time of a computational problem. The processors have independent instruction counters, meaning that each process ...
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-  L. M. Vidigal , S. R. Nassif , S. W. Director
Proceedings of the 23rd ACM/IEEE conference on Design automation July 1986
 The use of simulation tools to verify the behavior of integrated circuits is a well established technique for circuit design. This paper describes a novel approach for circuit simulation that promises a significant improvement over conventional methods. The algorithm involves an explicit event driven technique that seems stable even when the accuracy of the solution is relaxed, and is able to perform automatic and dynamic partitioning of the network, thus allowing the full exploitation of I ...
- 8** Proud: a fast sea-of-gates placement algorithm 80%
 Ren-Song Tsay , Ernest S. Kuh , Chi-Ping Hsu
Proceedings of the 25th ACM/IEEE conference on Design automation June 1988
 We present a fast and effective placement algorithm which takes advantage of inherent scarcity in the connectivity specification. It solves repeatedly sparse linear equations by the SOR (Successive Over-Relaxation) method in a top-down hierarchy. The algorithm has been implemented; for a triple-metal-layer 100K sea-of-gates design with 26,000 instances, it takes 50 minutes on a VAX 8650 and yields excellent results.
- 9** Design and analysis of power distribution networks in PowerPC microprocessors 80%
 Abhijit Dharchoudhury , Rajendran Panda , David Blaauw , Ravi Vaidyanathan , Bogdan Tutuianu , David Bearden
Proceedings of the 35th annual conference on Design automation conference May 1998
 We present a methodology for the design and analysis of power grids in the PowerPC™ microprocessors. The methodology covers the need for power grid analysis across all stages of the design process. A case study showing the application of this methodology to the PowerPC™ 750 microprocessor is presented.
- 10** Reduced-order modeling of large passive linear circuits by means of the SYPVL algorithm 80%
 R. W. Freund , P. Feldmann
Proceedings of the 1996 IEEE/ACM international conference on Computer-aided design January 1997
 Lucent Technologies This paper discusses the analysis of large linear electrical networks consisting of passive components, such as resistors, capacitors, inductors, and transformers. Such networks admit a symmetric formulation of their circuit equations. We introduce SyPVL, an efficient and numerically stable algorithm for the computation of reduced-order models of large, linear, passive networks. SyPVL represents the specialization of the more general PVL algorithm, to symmetric problems. Besid ...
- 11** Extraction of circuit models for substrate cross-talk 80%
 T. Smedes , N. P. van der Meijs , A. J. van Genderen
Proceedings of the 1995 IEEE/ACM international conference on Computer-aided design December 1995
 An increasingly urgent topic for the realization of densely packed (mixed signal) integrated circuits is prevention of cross-talk via the substrate. This paper proposes a Boundary Element Method (BEM) for calculating an admittance matrix for the substrate in order to analyze the parasitic coupling during layout verification. In contrast with standard BE methods, we propose a Green's function which is specific to the domain and the problem. This allows minimal discretization and a direct extractio ...
- 12** Automatic generation of optimization code based on symbolic non-linear domain formulation 80%
 Rainer Bacher
Proceedings of the 1996 international symposium on Symbolic and algebraic computation October 1996
- 13** Elaboration of the SEPT expert system as the coupling of a simulator and a diagnostician 77%
 Patrick Brézillon , D. Y. Bau , A. Hertz , A. P. Fauquembergue Maizener
Proceedings of the third international conference on Industrial and engineering applications of artificial intelligence and expert systems - Volume 1 June 1990
 We present the SEPT expert system which has been elaborated to resolve one of EDF's most crucial problems, namely the rapid processing of complex analysis for the repair and maintenance of EHV (Extra High Voltage) substations. In the first step, we implemented a prototype, which we called diagnostician, to validate the expert system approach. In the second step, a functional model of the system, known as the simulator, was developed to reinforce the diagnostician. The original nature of our ...
- 14** A network-variational basis for generalized computer representation of multifreedom, constrained, mechanical systems 77%
 Milton A. Chace
Proceedings of the 6th annual conference on Design Automation January 1969
 A vital component of computer-aided engineering design is the base program which computes the behavior of an arbitrary design, given a minimal input of both the structural identity and the design parameters. This paper considers the computer-aided design of multifreedom, constrained mechanical systems (realistic machinery). Characteristics of such systems and their computational representation and graphic display output are discussed in terms of an example machine system. An outline of math ...
- 15** Management information systems: Industrial production and digital computers 77%
 A. Holzman , O. I. Franksen , M. D. Romer
Proceedings of the 1965 20th national conference August 1965
 SOME OF THE MAIN problems in automating total data processing systems in industry, arise from the more complex problem areas. These areas include many of the so-called engineering design problems and also a majority of the higher level management decision processes in an industrial enterprise. These problem areas are normally dealt with by highly qualified personnel and are quite often presumed not to be automatable. The fact is that many theoretical schools are working on the development o ...

- 16** Computer-aided design of electrical circuits Simulation techniques (A Tutorial) 77%
 **Proceedings of the ACM '81 conference** January 1981
One of the very first applications of digital computers was that of simulation. Perhaps more computer time has been used over the years in this area than any other. Many programs are responsible for the largest computers in existence grinding away, day in and day out, in this general area. This paper will cover simulation as it applies to the design and development of Very Large Scale Integrated (VLSI) circuits. These techniques cover broadly the areas of process and circuit simu ...
- 17** An APL simulation of feedback systems 77%
 Wilbur R. LePage , Richard McFee
ACM SIGAPL APL Quote Quad , Proceedings of the international conference on APL July 1982
Volume 13 Issue 1
Practical feedback systems involve interacting linear and nonlinear components. Modern techniques of design are based on representing a feedback system by a set of first order nonlinear differential equations and using a digital computer to obtain experimental solutions. In this paper, APL notation is used in a concise development of the mathematical basis of a computing algorithm, and in the realization of an actual system which is effective from the standpoints of ease of use, complexity ...
- 18** An interactive test data system for LSI production testing 77%
 H. D. Schnurmann , R. M. Peters
Proceedings of the seventeenth design automation conference on Design automation June 1980
This paper describes a software system, ITDS, which supplies a chip or module tester with test data. There are two major components to the system: an interactive data entry system, ITLG; and a generator of environmental test data, SPEC/GEN. By "conversing" with its user, ITLG creates a technology library from a document of circuit specifications. The user does not need to be familiar with the tester. ITLG will guide the user by showing him how to enter the necessary data, by aud ...
- 19** Integrated manufacturing and development (IMaD) 77%
 David Moran , Daria Dooling , Tom Wilkins , Ralph Williams
Proceedings of the 1999 ACM/IEEE conference on Supercomputing (CDROM) January 1999
- 20** An empirical analysis of the performance of a multiprocessor-based circuit simulator 77%
 George K. Jacob , A. Richard Newton , Donald O. Pederson
Proceedings of the 23rd ACM/IEEE conference on Design automation July 1986
Our original MSPLICE multiprocessor-based circuit simulator showed excellent efficiency with up to 10 processors. As shown in this paper, however, the efficiency of the program drops significantly when over 40 processors are used. A new generation of the MSPLICE program is described which shows high efficiency with up to 99 processors for three different benchmark circuits. Data is compared against predictions made from simulations of an ideal Gauss-Seidel machine model with unit delay, and ...

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Randal E. Bryant , Michael Dd. Schuster

Proceedings of the 22nd ACM/IEEE conference on Design automation June 1985

This paper presents measurements obtained while performing fault simulations of MOS circuits modeled at the switch level. In this model the transistor structure of the circuit is represented explicitly as a network of charge storage nodes connected by bidirectional transistor switches. Since the logic model of the simulator closely matches the actual structure of MOS circuits, such faults as stuck-open and closed transistors as well as short and open-circuited wires can be simulated. By usi ...

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Yu-an Chen , Vikas Jha , Rajive Bagrodia

ACM SIGSIM Simulation Digest , Proceedings of the eleventh workshop on Parallel and distributed simulation June 1997
Volume 27 Issue 1

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Payam Heydari , Massoud Pedram

Proceedings of the 1998 international symposium on Physical design April 1998

In this paper, we present a new analytical approach for computing the ramp response of an RLC interconnect line with a pure capacitive load. The approach is based on the two-port representation of the transmission line and accounts for the output resistance of the driver and the line inductance. The results of our analysis are compared with the results of HSPICE simulations demonstrating the high accuracy of our solution under various values of driver, interconnect, and load impedan ...

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Scott Woods , Giorgio Casinovi



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This paper describes an algorithm for the simulation of gate-level logic. Multiple logic levels are used to describe the state of each node. Each state corresponds to a different voltage level, and the number of levels to be used for a simulation is user-defined. This feature

simplifies considerably the interface between a digital and an analog simulator. A DC solver is incorporated to find the initial operating point of a circuit before a transient analysis begins. This solver has the capabilit ...

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 Kieran L. Coughlan , Paul J. Nolan
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 Antonio Montes , Jordi Castro
ACM SIGSAM Bulletin January 1995
 Volume 29 Issue 1
 In Electrical Engineering one of the most important problems to be solved for electrical networks is the load flow problem [6] [3]. Currently numerical solutions are provided by Newton's method, which involves recomputing the solution whenever the input data change. Given that this problem must be solved very often with different input data, the Grobner basis can be an interesting approach since it can, in principle, provide a more algebraic solution of the input parameters and has to b ...
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 Diffusion is a well-known algorithm for load-balancing in which tasks move from heavily-loaded processors to lightly-loaded neighbors. This paper presents a rigorous analysis of the performance of the diffusion algorithm on arbitrary networks. It is shown that the running time of the diffusion algorithm is bounded by: $O(\log \frac{N}{F}) \leq \text{Time} \leq O(N \frac{N}{F})$ and $O(\log \frac{N}{F}) \leq \text{Time} \leq O(\frac{N}{F} \log N)$, where N is the number of no ...
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by a position-sensitive detector. A built-in **electric circuit** then calculates the distance to the object our method and test the accuracy through both **simulation** and measurement in a real robot environment. In case can be found in [10]3 Experiments 3.1 **Simulations** 1) Setup: We simulated a robot end-effector

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dissipation of energy across resistors in an **electric circuit**, passivity has been widely used in order to stabilization of a family of systems and present **simulations** to demonstrate the effectiveness of this controller. In section 4, we present a **simulation** to indicate the effectiveness of this approach.

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such a thermoelement is used as part of an **electric circuit**, it pumps heat from one junction to the One Dimensional **Simulation** for Peltier Current Leads Haruhiko Okumura

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 program The pilot used in this study is an **electric network** protection relay software. The relay itself
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and also by electrical resistance of the **electric network** naturally associated with graphs. There are Diaconis [20]The Brownian motion of a dust **particle** is random walk in the room. Models in <ftp.cs.yale.edu/WWW/HTML/YALE/CS/HyPlans/lovasz/erdos.ps>

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